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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,613	12/29/2003	Min-Suk Lee	51876P538	7503
8791	7590	09/02/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			VNH, LAN	
		ART UNIT	PAPER NUMBER	
		1765		

DATE MAILED: 09/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/748,613	LEE ET AL.
	Examiner Lan Vinh	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 December 2003.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3,6,7,9-16,19-20 and 22-25 is/are rejected.
 7) Claim(s) 4,5,8,17,18 and 21 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 6-7, 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,475,906) in view of Chang et al (US 2003/0066545A1)

Lee discloses a method for fabricating a DRAM integrated circuit. The method comprises the steps of:

forming a semiconductor substrate structure including a substrate 10, a nitride layer for forming a hard mask, a plurality of conductive patterns, an etch stop layer 34, an inter-layer insulation layer 40, an anti-reflective coating (ARC) layer 50 and a photoresist pattern 55 (col 3, lines 40-57)

selectively etching the ARC layer 50 and the nitride layer with use of the photoresist pattern 55 as an etch mask form a hard mask (col 3, lines 61-65; fig. 3)

removing the photoresist pattern and the ARC layer (as seen in fig. 3)

etching the inter-layer insulation layer disposed between the conductive patterns by using the hard mask as an etch mask to form a contact hole 42 exposing the etch stop layer 34 (col 3, lines 61-63)

removing the etch stop layer formed at a bottom area of the contact hole to expose the substrate (col 4, lines 1-2; fig. 3)

forming plug electrically contacted to the exposed substrate (col 5, lines 24-26)

Unlike the instant claimed invention as per claim 1, Lee fails to specifically disclose performing the etching steps in an in-situ condition

Chang discloses a method for reducing contamination after plasma etching comprises the step of performing the etching steps without breaking the vacuum between the chambers/ in an in-situ condition (col 2, paragraph 0021)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Lee method by performing the etching steps in an in-situ condition as per Chang because Chang discloses that different procedures performed in different chambers without breaking the vacuum provides uninterrupted process, thereby prevents contamination of wafers that often occurs when transferring wafers between various separate chambers (col 2, paragraph 0021)

Regarding claim 2, Lee discloses forming the conductive pattern has a stack structure including hard mask insulation layer and a conductive layer 27 (fig. 3)

The limitation of claim 3 has been discussed above

Regarding claim 6, Lee discloses forming the interlayer 40 of oxide (col 2, lines 61-63), performing a SAC etching step (col 3, lines 61-62)

Regarding claim 7, Lee discloses etching the SAC opening using an etching gas of C5F8 (col 3, lines 63-65)

Regarding claim 9, Lee discloses the step of forming a conductive material for forming the plug to make electrical contact to the exposed substrate, performing a planarizing

process/CMP process to polish the conductive material to expose the upper part of the conductive pattern (col 5, lines 21-31; fig. 9)

Regarding claim 10, Lee discloses depositing a metal layer on the surface of the substrate (col 5, lines 29-30)

Regarding claim 11, Lee discloses forming a photoresist pattern 55 in a hole type (fig. 2)

Regarding claim 12, Lee discloses forming gate electrode pattern (col 2, lines 55-56)

3. Claims 13-16, 19-20, 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US 6,475,906) in view of Chang et al (US 2003/0066545A1)

Lee discloses a method for fabricating a DRAM integrated circuit. The method comprises the steps of:

forming a semiconductor substrate structure including a substrate 10, a nitride layer for forming a hard mask, a plurality of conductive patterns, an etch stop layer 34, an inter-layer insulation layer 40, an anti-reflective coating (ARC) layer 50 and a photoresist pattern 55 (col 3, lines 40-57)

selectively etching the ARC layer 50 and the nitride layer with use of the photoresist pattern 55 as an etch mask form a hard mask (col 3, lines 61-65; fig. 3)

removing the photoresist pattern and the ARC layer (as seen in fig. 3)

etching the inter-layer insulation layer disposed between the conductive patterns by using the hard mask as an etch mask to form a contact hole 42 exposing the etch stop layer 34 (col 3, lines 61-63)

removing the etch stop layer formed at a bottom area of the contact hole to expose the substrate (col 4, lines 1-2; fig. 3)

forming plug electrically contacted to the exposed substrate (col 5, lines 24-26)

Unlike the instant claimed invention as per claims 13-14, Lee fails to specifically disclose loading the semiconductor substrate into an etching equipment having at least two chambers and performing the etching steps in an in-situ condition between the chambers

Chang discloses a method for reducing contamination after plasma etching comprises the step of loading the semiconductor substrate into an etching equipment having multiple chambers and performing the etching steps without breaking the vacuum between its chambers/ in an in-situ condition (col 2, paragraph 0021)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Lee method by loading the semiconductor substrate into an etching equipment having multiple chambers and performing the etching steps in an in-situ condition as per Chang because Chang discloses that different procedures performed in different chambers without breaking the vacuum provides uninterrupted process, thereby prevents contamination of wafers that often occurs when transferring wafers between various separate chambers (col 2, paragraph 0021)

Regarding claim 15, Lee discloses forming the conductive pattern has a stack structure including hard mask insulation layer and a conductive layer 27 (fig. 3)

The limitation of claim 16 has been discussed above

Regarding claim 19, Lee discloses forming the interlayer 40 of oxide (col 2, lines 61-63), performing a SAC etching step (col 3, lines 61-62)

Regarding claim 20, Lee discloses etching the SAC opening using an etching gas of C5F8 (col 3, lines 63-65)

Regarding claim 22, Lee discloses the step of forming a conductive material for forming the plug to make electrical contact to the exposed substrate, performing a planarizing process/CMP process to polish the conductive material to expose the upper part of the conductive pattern (col 5, lines 21-31; fig. 9)

Regarding claim 23, Lee discloses depositing a metal layer on the surface of the substrate (col 5, lines 29-30)

Regarding claim 24, Lee discloses forming a photoresist pattern 55 in a hole type (fig. 2)

Regarding claim 25, Lee discloses forming gate electrode pattern (col 2, lines 55-56)

Allowable Subject Matter

4. Claims 4-5, 8, 17-18, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 4, 17, the cited prior art of record, taken alone or in combination, fails to disclose a method for fabricating a semiconductor device comprises the step of

depositing the nitride layer with a predetermined thickness equal to or greater than the total thickness of lost portions of the hard mask insulation layer during the step (d) and the step (e), in combination with the rest of the limitations of claims 4, 17

Regarding claims 5, 18, the cited prior art of record, taken alone or in combination, fails to disclose a method for fabricating a semiconductor device comprises the step of removing the hard mask and the etch stop layer simultaneously, in combination with the rest of the limitations of claims 5, 18. The closest cited prior art of Lee discloses the step of removing the etch stop layer 34 without removing the hard mask layer 40 (fig. 3)

Regarding claims 8, 21, the cited prior art of record, taken alone or in combination, fails to disclose a method for fabricating a semiconductor device comprises the step of forming the ARC layer on the nitride layer, forming the photoresist pattern on the ARC layer through ArF photolithography, in combination with the rest of the limitations of claims 5, 18. The closest cited prior art of Lee discloses the step of forming the ARC layer 50 on the interlayer oxide layer 40 (fig. 2)

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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August 30, 2005